



(Foto: Audi AG)

# Use in development and production

**W**ith the introduction of the MOST150 compliance verification process for the physical layer, the MOST Cooperation has developed a test procedure, which reduces the number of components to be used. The signal generation and verification can essentially be covered with a single device: the Physical Layer Stress Test Tool (PhLSTT; figure 1). The measurement setup is complemented only by the usage of standard components, e.g. oscilloscope, light power meter, attenuator or mode mixer.

From the beginning, it was possible to create a standard successfully, that allows the highest possible uniformity for the verification of MOST150 control units in the physical layer – best preconditions for identical test processes and test results worldwide. The Physical Layer Stress Test Tool is a mandatory part of the compliance ve-

## Stress test tool for MOST150 physical layer

Performing a physical layer test for control units is simplified by using the Physical Layer Stress Test Tool. This covers essential functions such as generating a worst case pattern, signal conditioning, a pattern comparator and test procedure control. The high grade of transparency and efficiency for carrying out and analyzing physical layer test is also provided. Therefore, the foundations exist for the start of the compliance verification process for MOST control units.

From Georg Janker

rification and therefore it also plays a key role. This opens up the following areas of application for the PhLSTT:

- ▶ performing of the compliance process in the accredited test houses.
- ▶ accompanying development verification at the control unit manufacturers.

- ▶ quality assurance at the end-of-line in production.
- ▶ verification at the system integrators.

A physical layer test can be simplistically described by two definitions of tasks (figure 2): Applying worst case

scenarios for the control unit and verifying the signal produced by the DUT.

**Applying worst case scenarios for DUT**

The main task of the PhLSTT is to generate worst case patterns, which are applied to the control unit to be tested (so-called Device Under Test, DUT). By using a comparator, the output signal of the DUT is compared with the original pattern and then checked for errors.

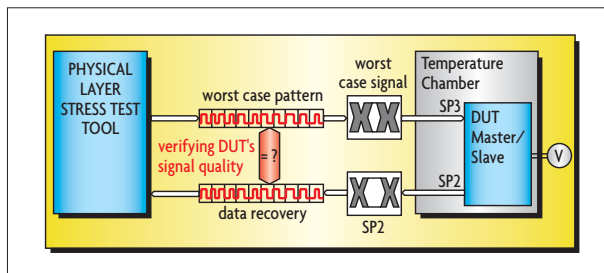


Figure 1. The Physical Layer Stress Test Tool (PhLSTT).

On the one hand, it can thus be determined if the DUT correctly interprets the bit sequence of the worst case pattern and, on the other hand, can also correctly output it again without violating the compliance standard. The worst case pattern scenario is combined with other stress conditions (e.g. temperature, supply voltage, light power) during compliance test execution.

**Signal quality check**

Verification of adherence to the signal quality under all possible conditions is the primary objective of the compliance verification. For this reason, it is also important to check whether the worst case signals are not only correctly received and interpreted, but also whether the control unit adheres at output (SP2 in figure 1) to the compliance requirements, also under these conditions (figure 3). For this purpose, in the measurement setup, in addition to the Physical Layer Stress Test Tool, an oscilloscope is combined in order, e.g. to check the eye diagram.

**Pattern generator and signal conditioner**

The pattern generator offers the possibility to apply a pattern at different

outputs of the PhLSTT. The pattern is generated by a high precision clock and optimized with a signal conditioner additionally – concerning to the pulse width. This reduces the transferred jitter to a minimum. Furthermore, the signal conditioner enables a deterministic adaptation of the duty cycle adjustment in high resolution.

The pattern can be picked off via different outputs on the PhLSTT alternatively: A commercially available FOT unit, a LVDS output operating with an external EOC or with the integrated High-Quality-EOC. The pattern – defined by the MOST Cooperation for the compliance process – is integrated in the unit by default. However, individual patterns can also be loaded via a communications interface.

**High-quality EOC**

A special feature of the integrated EOC is the high signal quality at maximum light power. The architecture of the EOC is also aligned to the pattern generator and signal conditioner, which enables a very accurate, reproducible signal.

As a result, a reference signal can be generated, which can be modified by means of additional components (such as e.g. optical attenuator or mode mixer), to fit the test scenario. An characteristic of the EOC is operation at more than +1 dBm, that enables the important test for compliance with maximum optical output power at the input of the DUT.

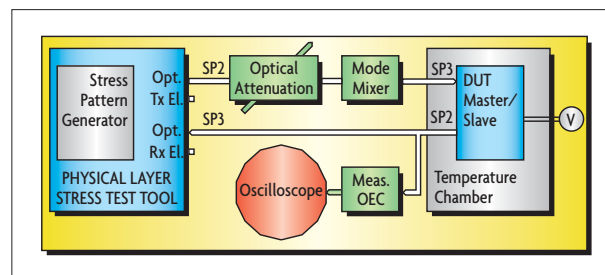


Figure 2. Physical layer testing scenario.

**Pattern comparator**

In addition to generation of the signal, it is important to check whether the pattern sent is also correctly recognized by the DUT (device under test) during the test execution. In order to be able to carry out this check, the DUT is set in a special bypass mode; the „Retimed Triggered Bypass Mode“. This mode forwards the received pattern in unmodified form. In this way, the pattern at the output of the DUT can be compared with the pattern applied from the PhLSTT. For this case a pattern comparator is implemented in the PhLSTT.

The pattern comparator can be switched to the integrated FOT unit as well as to an electrical input, which enables the connection of an external OEC. Various scenarios can thereby be realized such as e.g. the combination of an SP2 measurement and an oscilloscope. Analysis of the pattern comparator relates to two characteristics: The bit errors occurred and sudden phase shifts in the received signal. Both incidents are counted by the PhLSTT and reported after completion of the test. During the test, bit or phase errors that occurred can be more precisely located and analyzed via trigger outputs of the PhLSTT.

**Automation und test procedure**

The several steps, that are required for performing the test:

- ▶ Switching of the DUT to retimed triggered bypass mode: So that the DUT does not modify the signal in any way, it must be set to a so-called retimed triggered bypass mode. This takes place with the method Physical-LayerTest, which is called in the function block Enhanced Testability in the DUT.
- ▶ Switching of the PhLSTT to stress mode: In order to generate the pattern, the PhLSTT must be set from the normal MOST mode to pattern mode.

- ▶ Repeated sending of the pattern for a specific period of time: In the test phase, the pattern is cyclically sent for a predetermined period of time. A trigger output marks the start of the pattern in order to enable analyses with an oscilloscope during the test procedure.
- ▶ Pattern comparator operation: The pattern comparator is activated when it is ensured that the DUT and the PhLSTT are in the stress mode. From now on, all errors occurring – both in the DUT and in the pattern comparator – are counted.
- ▶ Switching to MOST mode: In order that the results can be compared after

the test, both DUT and PhLSTT have to switch back to normal MOST mode after a previously configured period of time.

- ▶ Readout of the results: The measured values of the unlock indicator and the error counter in the DUT are queried via the method PhysicalLayerTestResult provided by the function block Enhanced Testability.

The entire test procedure is carried out by the PhLSTT independently and automatically. The parameterization, the start of the test procedure and the results analysis are controlled via a se-

rial interface. An example program is provided with the PhLSTT. Therefore, performing a compliance test is possible immediately after completion of the test setup. *bg*



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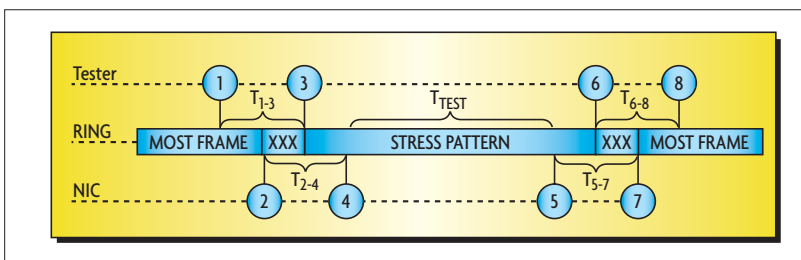


Figure 3. Typical measurement setup.